

## CLAIMS

1. A video signal conversion device converting an input video signal to a video signal suitable to a display device,

5 comprising:

a storage part storing the video signal;

*Full frame  
rate conversion*

10 a vertical frequency conversion processing circuit outputting a write control signal for writing the input video signal in said storage part and a read control signal for reading the video signal stored in said storage part to said storage part for controlling input/output of the video signal in/from said storage part while converting the vertical frequency of the video signal stored in said storage part;

15 an interlace-to-progressive conversion processing circuit converting, when the video signal output from said vertical frequency conversion processing circuit is an interlace signal, the video signal from the interlace signal to a progressive signal;

20 a scanning line conversion processing circuit converting the number of scanning lines of the video signal output from said interlace-to-progressive conversion processing circuit;

a horizontal pixel conversion processing circuit converting the number of horizontal pixels of the video signal output from said scanning line conversion processing circuit;

25 and

a synchronous control circuit outputting a synchronous control signal for controlling operations of said vertical frequency conversion processing circuit, said interlace-to-progressive conversion processing circuit, said scanning line conversion processing circuit and said horizontal pixel conversion processing circuit to said vertical frequency conversion processing circuit, said interlace-to-progressive conversion processing circuit, said scanning line conversion processing circuit and said horizontal pixel conversion processing circuit.

2. The video signal conversion device according to claim 1, wherein

said storage part includes a field memory,

said vertical frequency conversion processing circuit includes:

a first line memory performing a write operation with reference to a first clock output from said synchronous control circuit while performing a read operation with reference to a second clock output from said synchronous control circuit to perform write and read operations of said video signal in response to a horizontal synchronizing signal of a first system output from said synchronous control circuit, and

a vertical frequency conversion processing circuit operating with reference to said second clock for outputting

said write control signal in response to said horizontal synchronizing signal of said first system and a vertical synchronizing signal of a first system output from said synchronous control circuit while outputting said read control  
5 signal in response to a horizontal synchronizing signal of a second system and a vertical synchronizing signal of a second system output from said synchronous control circuit to convert the vertical frequency of the video signal output from said first line memory from the frequency of said vertical  
10 synchronizing signal of said first system to the frequency of said vertical synchronizing signal of said second system,

said interlace-to-progressive conversion processing circuit includes:

a second line memory operating with reference to said  
15 second clock for performing write and read operations of the video signal output from said vertical frequency conversion processing circuit in response to said horizontal synchronizing signal of said second system, and

an interlace-to-progressive conversion circuit  
20 operating with reference to said second clock for converting the video signal output from said second line memory from an interlace signal to a progressive signal in response to said horizontal synchronizing signal of said second system,

said scanning line conversion processing circuit  
25 includes:

a third line memory operating with reference to said second clock for performing a write operation of the video signal output from said interlace-to-progressive conversion circuit in response to said horizontal synchronizing signal of said second system while performing a read operation of the written video signal in response to a horizontal synchronizing signal of a third system output from said synchronous control circuit, and

a scanning line conversion circuit operating with reference to said second clock for converting the number of scanning lines of the video signal output from said third line memory in response to said horizontal synchronizing signal of said third system and said vertical synchronizing signal of said second system, and

said horizontal pixel conversion processing circuit includes:

a horizontal compression circuit operating with reference to said second clock for compressing the number of horizontal pixels of the video signal output from said scanning line conversion circuit in response to said horizontal synchronizing signal of said third system,

a fourth line memory performing a write operation with reference to said second clock while performing a read operation with reference to a third clock output from said synchronous control circuit to perform write and read

operations of the video signal output from said horizontal compression circuit in response to said horizontal synchronizing signal of said third system, and

a horizontal expansion circuit operating with reference  
5 to said third clock for expanding the number of horizontal pixels of the video signal output from said fourth line memory in response to said horizontal synchronizing signal of said third system.

10 3. The video signal conversion device according to claim 1, wherein

said storage part includes a field memory, and

said interlace-to-progressive conversion processing  
circuit includes a plurality of line memories so that the video  
15 signal is transferred from said field memory to at least one of said plurality of line memories in response to a delayed horizontal synchronizing signal lagging a horizontal synchronizing signal before interlace-to-progressive conversion in phase, for performing rotation of data between  
20 said plurality of line memories while performing synthesis of an interpolation line with data of said plurality of line memories and reading data of a current line from a line memory other than the line memory to which the video signal has been transferred among said plurality of line memories in response  
25 to said horizontal synchronizing signal.

4. The video signal conversion device according to claim 1,  
wherein

said storage part includes a field memory,

5       said vertical frequency conversion processing circuit  
includes:

an address generation circuit generating a reading start  
address larger than a writing start address of said field memory  
when increasing the number of scanning lines by said scanning  
10   line conversion processing circuit for performing vertical  
expansion processing while generating a reading start address  
of a negative number when reducing the number of scanning lines  
by said scanning line conversion processing circuit for  
performing vertical reduction processing, as the reading start  
15   address of said field memory, and

a black line insertion circuit inserting, when the  
reading start address of a negative number is generated by said  
address generation circuit, data of a black line by the value  
of the negative number,

20       said synchronous control circuit includes a horizontal  
synchronizing signal generation circuit reducing the frequency  
of a horizontal synchronizing signal in reading of said field  
memory when performing said vertical expansion processing  
while increasing the frequency of the horizontal synchronizing  
25   signal in reading of said field memory when performing said

vertical reduction processing, and

said vertical frequency conversion processing circuit controls the read operation of said field memory in response to the horizontal synchronizing signal output from said horizontal synchronizing signal generation circuit.

5 The video signal conversion device according to claim 1, wherein

said storage part includes a field memory,

10 said synchronous control circuit includes a determination circuit determining whether the video signal input in said vertical frequency conversion processing circuit is an odd field or an even field,

said vertical frequency conversion processing circuit includes a field information storage circuit storing field information determined by said determination circuit in response to a vertical synchronizing signal before vertical frequency conversion and reading the stored field information in linkage with the video signal stored in said field memory in response to the vertical synchronizing signal after vertical frequency conversion,

20 said vertical frequency conversion processing circuit outputs the video signal to said interlace-to-progressive conversion circuit in response to the field information read by said field information storage circuit, and

said interlace-to-progressive conversion processing circuit converts the video signal output from said vertical frequency conversion processing circuit from an interlace signal to a progressive signal by intra-field interpolation.

5

6. The video signal conversion device according to claim 1, wherein

said synchronous control circuit includes:

10 a first horizontal synchronizing signal generation circuit generating a horizontal synchronizing signal for creating a horizontal synchronizing signal forming the reference on the output side of said vertical frequency conversion processing circuit and on the input side of said scanning line conversion processing circuit,

15 a vertical synchronizing signal generation circuit generating a vertical synchronizing signal with the horizontal synchronizing signal generated from said first horizontal synchronizing signal generation circuit,

20 a second horizontal synchronizing signal generation circuit generating a horizontal synchronizing signal for creating a horizontal synchronizing signal forming the reference on the output side of said scanning line conversion processing circuit, and

25 a selection circuit receiving a vertical synchronizing signal created from a vertical synchronizing signal of the



video signal input in said vertical frequency conversion processing circuit and the vertical synchronizing signal output from said vertical synchronizing signal generation circuit for selecting and outputting the vertical synchronizing signal of said vertical synchronizing signal generation circuit when said vertical frequency conversion processing circuit performs vertical frequency conversion while selecting and outputting the vertical synchronizing signal created from the vertical synchronizing signal of the video signal input in said vertical frequency conversion processing circuit when said vertical frequency conversion processing circuit performs no vertical frequency conversion as a vertical synchronizing signal for creating a vertical synchronizing signal forming the reference on the output side of said vertical frequency conversion processing circuit and forming the reference on the output side of said scanning line conversion processing circuit, and

said first and second horizontal synchronizing signal generation circuits are reset with reference to the vertical synchronizing signal output from said selection circuit.

7. The video signal conversion device according to claim 6, wherein

said first horizontal synchronizing signal generation circuit includes a first counter generating a horizontal

synchronizing signal for creating a horizontal synchronizing signal forming the reference on the output side of said vertical frequency conversion processing circuit and on the input side of said scanning line conversion processing circuit,

5        said vertical synchronizing signal generation circuit includes a second counter dividing the frequency of the horizontal synchronizing signal generated from said first counter and generating a vertical synchronizing signal,

10        said second horizontal synchronizing signal generation circuit includes:

15        a third counter generating a horizontal synchronizing signal for creating a horizontal synchronizing signal forming the reference on the output side of said scanning line conversion processing circuit while outputting said horizontal synchronizing signal as a reference pulse for a PLL circuit generating a prescribed clock, and

20        a fourth counter deciding the dividing ratio of said PLL circuit, dividing the frequency of the clock output from said PLL circuit and generating a horizontal synchronizing signal for creating a horizontal synchronizing signal forming the reference on the output side of said horizontal pixel conversion processing circuit, and

25        said first and third counters are reset with reference to the vertical synchronizing signal output from said selection circuit.

8. The video signal conversion device according to claim 7,  
wherein

said fourth counter is reset with reference to the  
5 vertical synchronizing signal output from said selection  
circuit.

9. A video signal conversion method converting an input video  
signal to a video signal suitable to a display device with a  
10 storage part for storing the video signal, including:

a step of outputting a write control signal for writing  
the input video signal in said storage part and a read control  
signal for reading the video signal stored in said storage part  
to said storage part for controlling input/output of the video  
15 signal in/from said storage part while converting the vertical  
frequency of the video signal stored in said storage part;

a step of converting, when the video signal converted  
in said vertical frequency conversion step is an interlace  
signal, the video signal from the interlace signal to a  
20 progressive signal;

a step of converting the number of scanning lines of the  
video signal converted in said interlace-to-progressive  
conversion step;

a step of converting the number of horizontal pixels of  
25 the video signal converted in said scanning line conversion

step; and

a step of generating a synchronous control signal employed in respective said steps.

5 10. The video signal conversion method according to claim 9, wherein

said storage part includes a field memory,

said vertical frequency conversion step includes:

10 a step of performing write and read operations of said video signal in response to a horizontal synchronizing signal of a first system generated in said synchronous control signal generation step with a first line memory performing a write operation with reference to a first clock generated in said synchronous control signal generation step while performing  
15 a read operation with reference to a second clock generated in said synchronous control signal generation step, and

a step of outputting said write control signal in response to said horizontal synchronizing signal of said first system and a vertical synchronizing signal of a first system generated  
20 in said synchronous control signal generation step while outputting said read control signal in response to a horizontal synchronizing signal of a second system and a vertical synchronizing signal of a second system generated in said synchronous control signal generation step with a vertical  
25 frequency conversion circuit operating with reference to said

second clock to convert the vertical frequency of the video signal output from said first line memory from the frequency of said vertical synchronizing signal of said first system to the frequency of said vertical synchronizing signal of said  
5 second system,

said interlace-to-progressive conversion step includes:

a step of performing write and read operations of the video signal output from said vertical frequency conversion circuit in response to said horizontal synchronizing signal  
10 of said second system with a second line memory operating with reference to said second clock, and

a step of converting the video signal output from said second line memory from an interlace signal to a progressive signal in response to said horizontal synchronizing signal of  
15 said second system with an interlace-to-progressive conversion circuit operating with reference to said second clock,

said scanning line conversion step includes:

a step of performing a write operation of the video signal output from said interlace-to-progressive conversion circuit  
20 in response to said horizontal synchronizing signal of said second system while performing a read operation of the written video signal in response to a horizontal synchronizing signal of a third system generated in said synchronous control signal generation step with a third line memory operating with  
25 reference to said second clock, and

a step of converting the number of scanning lines of the video signal output from said third line memory in response to said horizontal synchronizing signal of said third system and said vertical synchronizing signal of said second system  
5 with a scanning line conversion circuit operating with reference to said second clock, and

said horizontal pixel conversion step includes:

a step of compressing the number of horizontal pixels of the video signal output from said scanning line conversion  
10 circuit in response to said horizontal synchronizing signal of said third system with a horizontal compression circuit operating with reference to said second clock,

a step of performing write and read operations of the video signal output from said horizontal compression circuit  
15 in response to said horizontal synchronizing signal of said third system with a fourth line memory performing a write operation with reference to said second clock while performing a read operation with reference to a third clock generated in said synchronous control signal generation step, and

20 a step of expanding the number of horizontal pixels of the video signal output from said fourth line memory in response to said horizontal synchronizing signal of said third system with a horizontal expansion circuit operating with reference to said third clock.

11. The video signal conversion method according to claim 9,  
wherein

said storage part includes a field memory, and

said interlace-to-progressive conversion step includes  
5 a step of employing a plurality of line memories and  
transferring the video signal to at least one of said plurality  
of line memories from said field memory in response to a delayed  
horizontal synchronizing signal lagging a horizontal  
synchronizing signal before interlace-to-progressive  
10 conversion in phase for performing rotation of data between  
said plurality of line memories while performing synthesis of  
an interpolation line with data of said plurality of line  
memories for reading data of a current line from one line memory  
other than the line memory to which the video signal has been  
15 transferred among said plurality of line memories in response  
to said horizontal synchronizing signal.

12. The video signal conversion method according to claim 9,  
wherein

20 said storage part includes a field memory,

said vertical frequency conversion step includes:

a step of generating a reading start address larger than  
a writing start address of said field memory when increasing  
the number of scanning lines in said scanning line conversion  
25 step for performing vertical expansion processing while

generating a reading start address of a negative number when reducing the number of scanning lines in said scanning line conversion step for performing vertical reduction processing, as the reading start address of said field memory, and

5 a step of inserting, when the reading start address of a negative number is generated in said address generation step, data of a black line by the value of said negative number,

said synchronous control signal generation step includes a step of reducing the frequency of the horizontal synchronous signal in reading of said field memory when performing said vertical expansion processing while increasing the frequency of the horizontal synchronizing signal in reading of said field memory when performing said vertical reduction processing, and

10 said vertical frequency conversion step includes a step of controlling the read operation of said field memory in response to the horizontal synchronizing signal output in said synchronous control signal generation step.

13. The video signal conversion method according to claim 9,  
20 wherein

said storage part includes a field memory,

said synchronous control signal generation step includes a step of determining whether the video signal input in said vertical frequency conversion step is an odd field or an even  
25 field,



said vertical frequency conversion step includes a step of storing field information determined in said determination step in response to a vertical synchronizing signal before vertical frequency conversion and reading the stored field information in linkage with the video signal stored in said field memory in response to the vertical synchronizing signal after vertical frequency conversion,

said vertical frequency conversion step includes a step of outputting the video signal in response to the read field information, and

said interlace-to-progressive conversion step includes a step of converting the video signal output in response to said field information from an interlace signal to a progressive signal by intra-field interpolation.

14. The video signal conversion method according to claim 9, wherein

said synchronous control signal generation step includes:

a step of generating a horizontal synchronizing signal for creating a horizontal synchronizing signal forming the reference on the output side in said vertical frequency conversion step and on the input side in said scanning line conversion step with a first horizontal synchronizing signal generation circuit,

a step of generating a vertical synchronizing signal with the horizontal synchronizing signal generated from said first horizontal synchronizing signal generation circuit with a vertical synchronizing signal generation circuit,

5 a step of generating a horizontal synchronizing signal for creating a horizontal synchronizing signal forming the reference on the output side in said scanning line conversion step with a second horizontal synchronizing signal generation circuit,

10 a step of receiving a vertical synchronizing signal created from a vertical synchronizing signal of the video signal on the input side in said vertical frequency conversion step and the vertical synchronizing signal output from said vertical synchronizing signal generation circuit for selecting and outputting the vertical synchronizing signal of said  
15 vertical synchronizing signal generation circuit when performing vertical frequency conversion in said vertical frequency conversion step while selecting and outputting the vertical synchronizing signal created from the vertical  
20 synchronizing signal of the video signal on the input side in said vertical frequency conversion step when performing no vertical frequency conversion in said vertical frequency conversion step as a vertical synchronizing signal for creating a vertical synchronizing signal forming the reference on the  
25 output side in said vertical frequency conversion step and

forming the reference on the output side in said scanning line conversion step, and

a step of resetting said first and second horizontal synchronizing signal generation circuits with reference to the  
5 vertical synchronizing signal selected in said selection step.

15. The video signal conversion method according to claim 14, wherein

said step of generating the horizontal synchronizing  
10 signal with said first horizontal synchronizing signal generation circuit includes a step of generating a horizontal synchronizing signal for creating a horizontal synchronizing signal forming the reference on the output side in said vertical frequency conversion step and on the input side in said scanning  
15 line conversion step with a first counter,

said step of generating the vertical synchronizing signal with said vertical synchronizing signal generation circuit includes a step of dividing the frequency of the horizontal synchronizing signal generated from said first  
20 counter and generating a vertical synchronizing signal with a second counter,

said step of generating the horizontal synchronizing signal with said second horizontal synchronizing signal generation circuit includes:

25 a step of generating a horizontal synchronizing signal

for creating a horizontal synchronizing signal forming the reference on the output side in said scanning line conversion step while generating said horizontal synchronizing signal as a reference pulse for a PLL circuit generating a prescribed  
5 clock with a third counter, and

a step of deciding the dividing ratio of said PLL circuit, dividing the frequency of the clock output from said PLL circuit and generating a horizontal synchronizing signal for creating a horizontal synchronizing signal forming the reference on the  
10 output side in said horizontal pixel conversion step with a fourth counter, and

said step of resetting said first and second horizontal synchronizing signal generation circuits includes a step of resetting the first and third counters with reference to the  
15 vertical synchronizing signal selected in said selection step.

16. The video signal conversion method according to claim 15, wherein

said step of resetting said first and second horizontal  
20 synchronizing signal generation circuits further includes a step of resetting said fourth counter with reference to the vertical synchronizing signal selected in said selection step.